

CPS104 Homework-5

Due: November 2 (Hand in on paper in class) **Single cycle processor.**

1. We wish to add the instruction **jal** (a function call) to the single cycle data-path described in class (See also Figures 1 & 2). Add any necessary data-path components and controls signals necessary to figures 1 & 2 to make it possible for the data-path to execute **jal** in addition to all the instructions in the subset.
2. This is similar to problem 1, except that we wish to add the instruction **bne**.
3. This is similar to problem 1 except that we wish to add a modified version of **lw** that sums up the content of two register to obtain the address of the data to be loaded and uses the R-format.
4. Consider the single clock cycle per instruction implementation of the MIPS processor shown in figures 1-2. The **ALUctr0**, **ALUctr1** and **ALUctr2** bits control the ALU in the following manner:

ALU Operation	ALUctr0	ALUctr1	ALUctr2
A + B	0	0	0
A - B	0	0	1
A AND B	0	1	0
A OR B	0	1	1
A XOR B	1	0	0
A NOR B	1	0	1
A NAND B	1	1	0
NOT B	1	1	1

ExtOp=0 means a zero-extend and **ExtOp=1** means sign-extend.

Show the control values for the following instructions:

```
addi $s1, 0x1000
beq  $s1, $s2, L1
andi $s1, 0xffff
sub  $s1, $s2, $s3
sw   $s1, 100($s2)
```

Control Signal	addi	beq	andi	sub	sw
RegDst					
ALUsrc					
MemtoReg					
RegWr					
MemWr					
Branch					
Jump					
ExtOp					
ALctr0					
ALUctr1					
ALUctr2					

Figure 1: Datapath

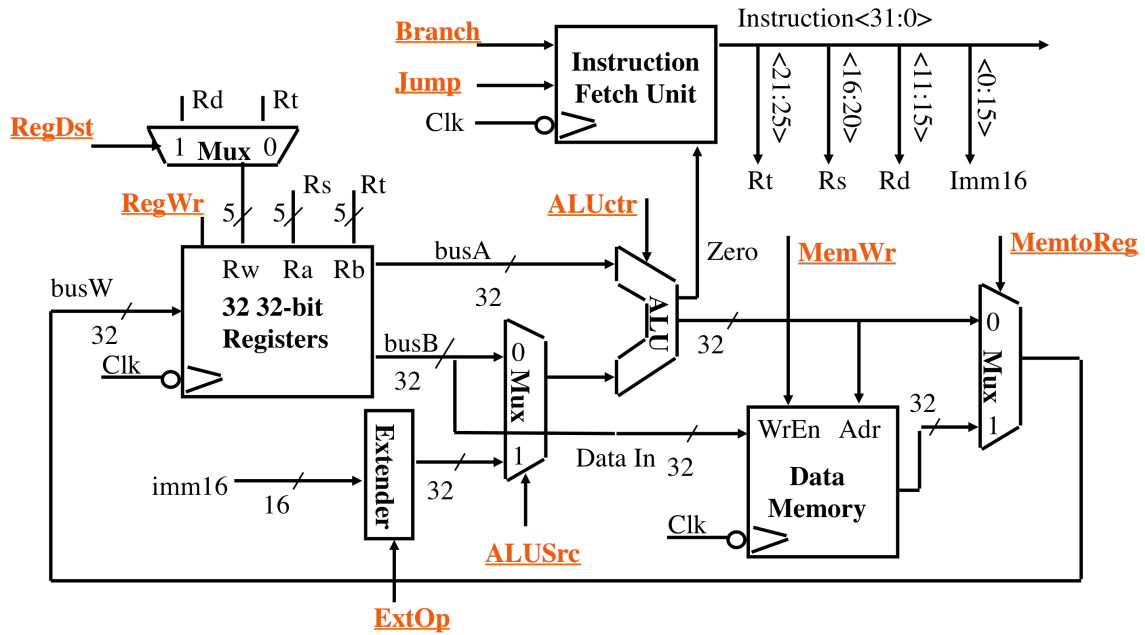


Figure-2 Instruction Fetch Unit

