

CPS 104 Final Exam

Fall 2001

Closed Book, 3 hours.

Answer all questions. State all your assumptions; clearly mark your final answers.

Please make sure that your exam has all 12 pages (including a blank page and the figure page.)

Write your name on each page of the exam.

Read all questions and use your time accordingly.

If you need more space, use the pages' backside. Make sure to write your name on any additional pages you use. Label each continuation.

Good Luck!

Your Name: _____

Problem 1: (20 pt) _____

Problem 2: (10 pt) _____

Problem 3: (30 pt) _____

Problem 4: (20 pt) _____

Problem 5: (10 pt) _____

Problem 6: (20 pt) _____

Problem 7: (15 pt) _____

Problem 8: (15 pt) _____

Total: (140 pt) _____

1. The MIPS assembler and instruction set (20 pt)

a. (6 pt) Explain what are assembler pseudoinstructions and their relations to “native” MIPS instructions.

b. (7 pt) Explain why

```
ori $s0, 0x7256ab20
```

can't be a “native” MIPS instruction

c. (7 pt) Translate the instruction

```
li $s0, 0x7256ab20
```

into equivalent “native” MIPS instruction(s).

2. Single Cycle per Instruction Processor (10 pt)

Consider the single clock cycle per instruction implementation of the MIPS processor shown in figure-1 (at the back of the exam). $ALUctr0$, $ALUctr1$ and $ALUctr2$ bits control the ALU in the following manner:

ALU Operation	ALUctr0	ALUctr1	ALUctr2
A + B	0	0	0
A - B	0	0	1
A AND B	0	1	0
A OR B	0	1	1
A XOR B	1	0	0
A NOR B	1	0	1
A NAND B	1	1	0
NOT B	1	1	1

$ExtOp=0$ means a zero-extend and $ExtOp=1$ means sign-extend.
Show the control values for the following instructions:

```
addi $s1, 0x1000
beq  $s1, $s2, L1
andi $s1, 0xffff
sub  $s1, $s2, $s3
sw   $s1, 100($s2)
```

Control Signal	addi	beq	andi	sub	sw
RegDst					
ALUsrc					
MemtoReg					
RegWr					
MemWr					
Branch					
Jump					
ExtOp					
ALctr0					
ALUctr1					
ALUctr2					

3. Cache Memory Organization (30 pt)

- a. (15 pt) Draw a block diagram of an 8 kilobyte 2-way set associative cache with 32 byte blocks. Explain the meaning of each field in the cache. Clearly show how an address from the CPU is used to determine if the block is resident. Indicate what address bits are used for each task.

- b. (15 pt) Assume a 16 entries direct mapped cache with 16 byte blocks and initial content of the tag array shown below:
- ii) (5 pt) Label each of the 10 memory accesses that occur in the order shown as a hit or a miss.
 - iii) (5 pt) Show the content of the tag array after the 10 memory accesses occur.
 - iv) (5 pt) What is the memory address (in hex) of the second word of the block that resides in Index 7 of the cache after the 10 memory accesses occur?

Index	Initial Tag	Final Tag
0	0x003abf	
1	0xffe123	
2	0x00045a	
3	0x00045a	
4	0xfffe00	
5	0xfffe01	
6	0x4ab2ab	
7	0x00045a	
8	0xa4112b	
9	0x000111	
10	0xfffe9a	
11	0x0ab100	
12	0x0ab101	
13	0xfffe01	
14	0xffe123	
15	0x00045b	

Memory access address	Hit/Miss
0x00001aec	_____
0x000011ec	_____
0xfffe9aa4	_____
0x003bbf08	_____
0x003abf14	_____
0xfffe9aac	_____
0xfffe9abc	_____
0x000011e0	_____
0x00045b80	_____
0xffe123e8	_____

The address of the nd2 word of the block that resides in Index=7 is:

0x_____

4. Virtual Memory (20 pt)

a. (5 pt) What is a page table and what is the TLB?

b. (5 pt) Why is the TLB needed?

c. (5 pt) What is the difference between a page fault and a TLB miss?

d. (5 pt) Assuming a virtual memory system with 4KB pages. What 28-bit physical address (in Hex) does the 32-bit virtual address 0x045aab14 map to, given the four entry fully associative TLB shown below:

V	Acc	D	Virtual	Physical
1	rw	0	0x0345a	0x0022
1	rw	1	0x0045a	0x7fff0
1	rw	1	0x045aa	0xafc7
1	rw	0	0xab144	0x0023

Physical Address: _____

5. Interrupts (10 pt)

a. (5 pt) What are interrupts and exceptions? What are they used for?

b. (5 pt) Give examples for interrupts or exceptions that are generated by:

i. Intentionally by a user program.

ii. Unintentionally by a user program.

ii. By a memory access.

iii. By an I/O device.

6. Input/Output (20 pt)

a. (10pt) What is bus arbitration and when is it needed?

i) (10 pt) Draw diagrams for centralized arbitration and daisy chain arbitration schemes. Explain the advantages and disadvantages of each.

7. Binary Arithmetic (15 points)

a) What decimal numbers the following two's complement numbers represent. Please note, when appropriate, you can give your answer as an expression rather than as a number!

i) 1111 1111 1111 1111 1111 1110 0000 1100 ?

ii) 1111 1111 1111 1111 1111 1111 1111 1111 ?

iii) 0111 1111 1111 1111 1111 1111 1111 1111 ?

b) What binary number does this hexadecimal number represent:

0x7fffffff

c) What hexadecimal number does this binary number represent:

1100 1010 1111 1110 1111 1010 1011 1101 ?

8. (15 points)

a. Write down the truth table for 2-bit by 2-bit multiply unit (four bits results).

b. Draw a circuit that implements the multiplier.

