

CPS104 Exam Practice Questions

1. Here is a list of address references given as *word* addresses: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17, 16. Assuming a direct mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss. Show the final content of the cache.

2. Using the same reference sequence given in problem 1, label each reference in the list as a hit or a miss and show the final content of the cache of a direct mapped cache with four-word cache blocks *and a total size of 16 words*.

3. Using the same reference sequence given in problem 1, label each reference in the list as a hit or a miss and show the final content of the cache of a two-way set associative cache with one-word cache blocks *and a total size of 16 words*.

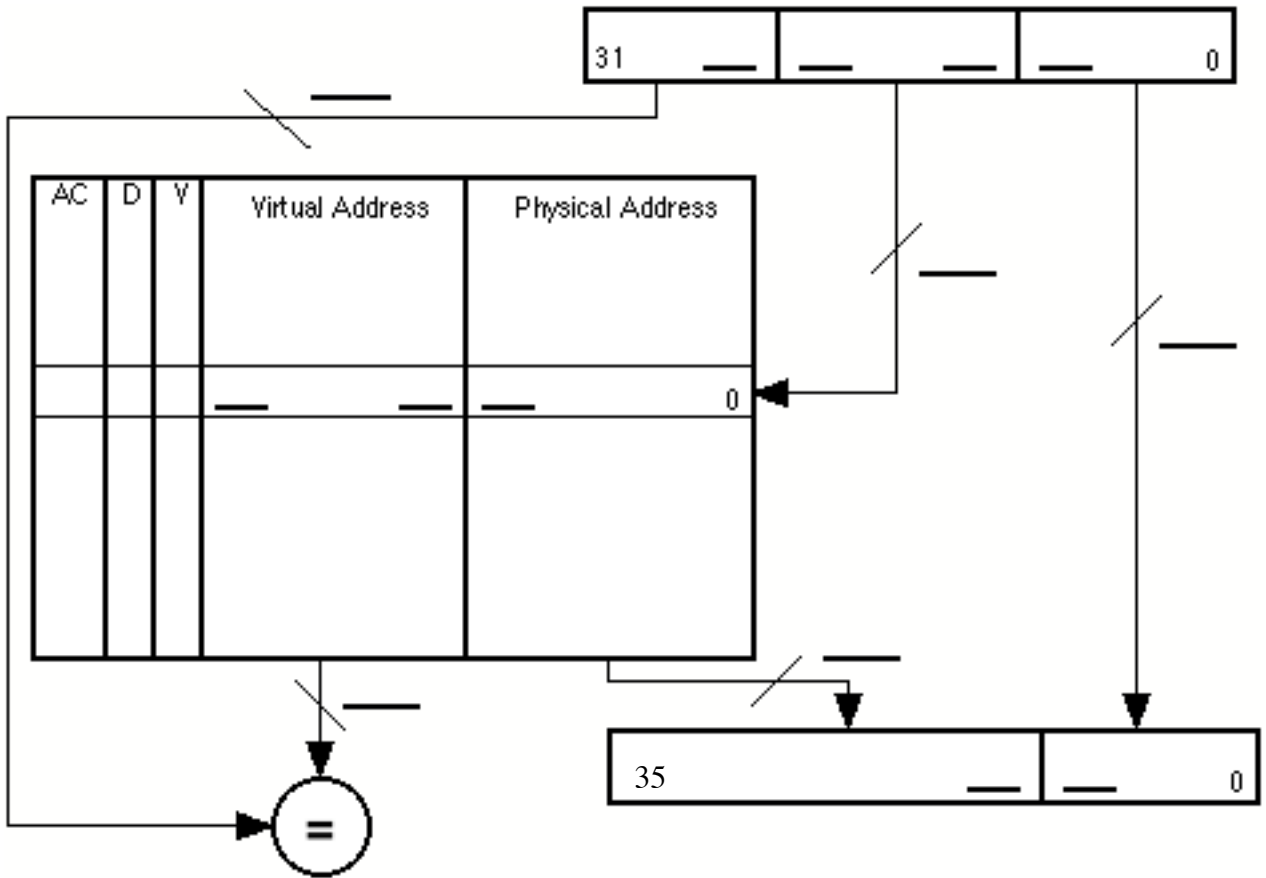
4. The following C++ program is run on a machine with a cache that has four-word (16 bytes) blocks and holds 256 bytes of data.

```
int i, j, c, stride, array[256];
. . .
for (I=0; I<1000; I++)
    for(j=0; j < 256; j = j+stride)
        c = c+array[j] ;
```

If we consider only cache activity generated by references to the array, what is the expected miss rate when the cache is direct mapped and `stride=132`? How about if `stride=131`? Would either of these change if the cache were two-way set associative?

5. Assume a virtual memory system with 32-bit virtual addresses, 36-bit physical addresses, 4K-byte pages and 64-entry direct-mapped translation lookaside buffer (TLB).

- a. Describe how a translation lookaside buffer works and what happens on both TLB hits and misses.
- b. Label the attached picture of the TLB to show which bits are used to index the TLB, which bits are involved in the comparisons and which bits are used to form the physical address. Label each of the signals (lines) to indicate how many bits are passed. For the fields in the TLB, show which bits of the virtual and physical address are stored in each field. Be sure to write you numbers in the space provided.



6. Assume a virtual memory system with 32-bit virtual addresses, 28-bit physical addresses, 4K-byte pages and 16-entry fully associative translation look-aside buffer (TLB).
 - a. Describe how a translation look-aside buffer works and what happens on both TLB hits and misses.

b. The TLB described in part a. contains:

AC	V	Virtual	Physical
rw	1	0x12345	0x2a45
rw	1	0x047e4	0x2a46
rw	1	0x047f0	0x1e45
rw	1	0x0047f	0x1e46
rw	1	0x047ef	0x1e47
rw	1	0xf1e45	0x1e48
rw	1	0x047f1	0x2a47
rw	1	0x047f2	0x1e4a
rw	1	0x047e5	0x4e44
rw	1	0x047e3	0x4e43
rw	1	0xf1e46	0x2a43
rw	1	0x04fe4	0x0e45
rw	1	0x004fe	0x0e46
rw	1	0x47f10	0x00af
rw	1	0x47f1e	0x047f
rw	1	0x47f1f	0x47f1

To what physical addresses the virtual addresses below translate to? Write your answer in Hex.

Virtual address	physical address
0x047f1e45	
0x004fe245	
0x047f20e3	
0x047e4234	
0x47f1f234	

7. Assume your computer has a 16KB direct mapped cache with 32-byte cache blocks. Consider the following C++ code fragment:

```

int index[1000];
double altitude[1000];
int i;

.
.
.

for (i=0; i < 1000; i = i +12)
    if ( index[i] < 112) altitude[i] = altitude[i]* 2.0;
    else altitude[i] = altitude[i]/2.0;

```

Assume that at the start of the **for** loop the cache is empty.

a. How many cache-misses would result by executing the above loop?

b. Reorganize the data structures (**index** and **altitude**) and rewrite the loop so your new code will perform the *same computation* but will have improved cache behavior. Explain why the new code will perform better.

8. Interrupts:

a. What are interrupts exceptions and traps? What are they used for?

b. Give an example of an interrupt or an exception that is generated:

i. Intentionally by the operating system.

ii. Unintentionally by a user program.

iii. By a memory access.

iv. By an I/O device.

9. What is a DMA device? What is it used for?

10. Compare and contrast Centralized arbitration to daisy-chaining.